MBA-506A0
VLSI
80286 6/12/16 MHZ
BABY AT MAINBOARD
USER'S MANUAL

TABLE OF CONTENTS

WHAT WE POSSESS THAT OTHERS WITHOUT!

* 5 chips set full CMOS process low power consumption
* Norton SI benchmark rating of 16.0
* Zero wait state read operations
* One wait state write operations
* 20 mA, 200pF slot drive (system bus) capability
* 8 mA, 150pF DRAM drive capability
* Four layer implementation for low noise operation

I. SPECIFICATION

GENERAL SPECIFICATION

* Intel or AMD 80286 10MHz or 12MHz CPU
* 6/8/12/16MHz speed hardware and software selectable
* RAM access time 0-wait and 1-wait switchable
* Up to 4 mega byte memory on board
* 16 mega byte expandable memory in the protect virtual address mode
* 2 sockets for AMI, PHOENIX or AWARD BIOS, fully compatible with IBM BIOS
* 8 I/O expansion slots
* Socket for 80287 math processor
* CMOS clock and calendar circuit with rechargable battery support
* 24-bit addressing and 16-bit data path capabilities
* 16-level interrupts
* 7-channel DMA (Direct memory access)
* 3-programmable timers

SYSTEM MEMORY MAP

ADDRESS RANGE	START-END	NAME	FUNCTION
000000-03FFFF	000K-256K	Bank 0	System memory (256K)
040000-07FFFF	256K-512K	Bank 1	System memory (256K)
080000-09FFFF	512K-640K	Bank 2	System memory (128K)
0AFFFF-0BFFFF	640K-768K	Video	Display card buffer (128K)
0C0000-0DFFFF	768K-896K	I/O ROM	Expansion ROM (128K)
0E0000-0EFFFF	896K-960K	ROM	System usage (64K)
0F0000-0EFFFF	960K-1024K	ROM	BIOS (64K)
100000-11FFFF	1024K-1152K	Bank 2	System memory (128K)
120000-15FFFF	1152K-1408K	Bank 3	System memory (128K)
160000-FDFFFF	1408K-16146K	RAM	Expansion RAM (14870K)
FE0000-FEFFFF	16146K-16210K	ROM	System usage (64K)
FF0000-FFFFFF	16210K-16274K	ROM	BIOS (64K)

I/O CHANNEL SLOTS

The I/O channel supports:

* I/O address space hex 100 to hex 3FF
* 24-bit memory addresses (16MB)
* Refresh of system memory from channel microprocessors
* Selection of data accesses (eigher 8 bit or 16 bit)
* Interrupt
* DMA channels
* I/O wait-state generation
* Open-bus structure (allowing multiple microprocessors to share the system's resources, including memory)

I/O ADDRESS MAP

HEX RANGE	DEVICES	USAGE
000-01F	DMA controller 1	System
020-03F	Interrupt controller 1	System
040-05F	Timer	System
060-06F	8042 (Keyboard)	System
070-07F	Real time clock, NMI mask	System
080-09F	DMA page register	System
0A0-0BF	Interrupt controller 2	System
0C0-0DF	DMA controller 2	System
0F0	Clear Math Coprocessor busy	System
0F1	Reset Math Coprocessor	System
0F8-0FF	Math Coprocessor	System
1F0-1F8	Fixed disk	I/O
200-207	Game I/O	I/O
278-27F	Parallel printer port 2	I/O
2F8-2FF	Serial port 2	I/O
300-31F	Prototype card	I/O
360-36F	Reserved	I/O
378-37F	Parallel printer port 1	I/O
380-38F	SDLC, bisynchronous 2	I/O
3A0-3AF	Bisynchronous 1	I/O
3B0-3BF	Monochrome display and printer adapter	I/O
3C0-3CF	Reserved	I/O
3D0-3DF	Color/graphic monitor adapter	I/O
3F0-3F7	Floppy diskette controller	I/O
3F8-3FF	Serial port 1	I/O

Numbering of the I/O slots is as follows:

REARPANEL

GND	B1	I	I	A1	–I/O CH CK
RESET DRV	B2	I	I	A2	SD7
+5Vdc	B3	I	I	A3	SD6
IRQ2	B4	I	I	A4	SD5
–5Vdc	B5	I	I	A5	SD4
DRQ2	B6	I	I	A6	SD3
–12VDc	B7	I	I	A7	SD2
0WS	BB	I	I	A8	SD1
+12Vdc	B9	I	I	A9	SD0
GND	B10	I	I	A10	–I/O CH RDY
–SMEMW	B11	I	I	A11	AEN
–SMEMR	B12	I	I	A12	SA19
–IOW	B13	I	I	A13	SA18
–IOR	B14	I	I	A14	SA17
–DACK3	B15	I	I	A15	SA16
DRQ3	B16	I	I	A16	SA15
–DACK1	B17	I	I	A17	SA14
DRQ1	B1B	I	I	A18	SA13
–REFRESH	B19	I	I	A19	SA12
CLK	B20	I	I	A20	SA11
IRQ7	B21	I	I	A21	SA10
IRQ6	B22	I	I	A22	SA9
IRQ5	B23	I	I	A23	SA8
IRQ4	B24	I	I	A24	SA7
IRQ3	B25	I	I	A25	SA6
–DACK2	B26	I	I	A26	SA5
T/C	B27	I	I	A27	SA4
BALE	B2B	I	I	A28	SA3
+5Vdc	B29	I	I	A29	SA2
OSC	B30	I	I	A30	SA1
GND	B31	I	I	A31	SA0

REARPANEL

–MEM CS16	D1	I	I	C1	SBHE
–I/O CS16	D2	I	I	C2	LA23
IRQ16	D3	I	I	C3	LA22
IRQ11	D4	I	I	C4	LA21
IRQ12	D5	I	I	C5	LA20
IRQ15	D6	I	I	C6	LA19
IRQ14	D7	I	I	C7	LA18
–DACK0	D8	I	I	C8	LA17
DRQ0	D9	I	I	C9	–MEMR
–DACK5	D10	I	I	C10	–MEMW
DRQ5	D11	I	I	C11	SD08
–DACK6	D12	I	I	C12	SD09
DRQ6	D13	I	I	C13	SD10
–DACK7	D14	I	I	C14	SD11
DRQ7	D15	I	I	C15	SD12
+5Vdc	D16	I	I	C16	SD13
–MASTER	D17	I	I	C17	SD14
GND	D18	I	I	C18	SD15

II. MAIN BOARD JUMPER SELECTION

CONNECTORS AND JUMPERS

The system board has the following connectors and jumpers:

JUMPER NUMBER	FUNCTION
JP1	EPROM size selection
JP2	RAM size selection
JP3	RAM size selection
JP4	RAM size selection
JP5	Not use
JP6	6/12 or 8/12 MHz selection
JP7	Display adapter selection
JP8	I/O wait selection

Below is a list of the Jumper Location.

JP1: EPROM size selection

Jumper JP1 is used to select ROM size of either 27256 or 27128 chip. Under normal operating conditions, you should not change these settings.

Pin 1,2	ON	27256
Pin 2,3	ON	27128

JP2, JP3, JP4 RAM size selection

Jumpers are used together to allow you to select the amount of RAM on board. See the table below for the connecting position. Jumper settings:

	Bank 0	Bank 1	JP2	JP3	JP4
1	4MB 41C000x18	41C000x18	OFF	ON	ON
2	2MB 41C000x18	None	ON	OFF	OFF
3	1MB 41256x18	41256x18	ON	OFF	ON
4	640KB 41256x18	4164x18	ON	ON	OFF
5	512KB 41256x18	None	ON	ON	ON

JP6: 6/12MHz or 8/12MHz selection

Jumper JP6 is used to select the speed mode, to select the 8/12 MHz mode, place a jumper cap over JP6

JP7: Monitor selection

Jumper JP7 is used to select a monochrome or a color graphic primary display adapter.

Jumper setting: To select the monochrome primary adapter, place a jumper cap over JP7 to select the color primary adapter, remove the jumper cap from JP7

JP8: One/zero-wait selection

Jumper JP8 is used to select 0-wait state in read operation, place a jumper cap over JP8. To select the one-wait state, remove a jumper cap from JP8.

Speaker connector

Its pin assignments are as follows:

PIN	ASSIGNMENT
1	Data out
2	Not used
3	GND
4	+5Vdc

External battery connector

The connector is for connecting four size "AA" batteries instead of the blue barrel shaped rechargable battery. Its pin assignments are as follows:

PIN	ASSIGNMENT
1	6Vdc
2	Not used
3	GND
4	GND

Keylock/Power LED

The power LED and Keylock connector is a 5 pin berg strip. Its pin assignments are as follows:

PIN	ASSIGNMENT
1	Power LED
2	Not used
3	GND
4	Keyboard inhibit
5	GND

Power supply connector

PIN	ASSIGNMENT	WIRE COLOR
1	Power good	Orange
2	+5V	Red
3	+12V	Yellow
4	–12V	Blue
5	GND	Black
6	GND	Black

PIN	ASSIGNMENT	WIRE COLOR
1	GND	Black
2	GND	Black
3	–5V	White
4	+5V	Red
5	+5V	Red
6	+5V	Red

Keyboard connector

The keyboard connector is a 5-pin, 90-degree printed circuit board (PCB) mounting, DIN connector. The assignments are as follows:

PIN	ASSIGNMENT
1	Keyboard clock
2	Keyboard ata
3	Not used
4	GND
5	+5V

IV. HARDWARE COMPATIBILITY

SYSTEM TIMERS

The system has three programmable timer/counters controlled by an Intel 8254-2 timer/counter chip. These are channels 0 through 2, defined as follows:

Channel 0	System Timer
GATE 0	Tied on
CLK IN 0	1.190 MHz OSC
CLK OUT 0	8259A IRQ

Channel 1	Refresh Request Generator
GATE 1	Tied on
CLK IN 1	1.190 MHz OSC
CLK OUT 1	Request Refresh Cycle

Note: Channel 1 is programmed to generate a 15 microsecond period signal.

Channel 2	Tone Generation for Speaker
GATE 2	Controlled by bit 0 of port hex 61 PPI bit
CLK N 2	1.190 MHz SOC
CLK OUT 2	Used to drive the speaker

SYSTEM INTERRUPTS

Sixteen levels of system interrupts are provided by the 80286 NMI and two 8259A Interrupt Controller chips. The following shows the interrupt-level assignments in decreasing priority:

LEVEL	FUNCTION
Microprocessor NMI	Parity or I/O channel check
Interrupt controllers CTRL 1 CTRL 2	
IRQ 0	Timer output 0
IRQ 1	Keyboard (Output buffer full)
IRQ 2 ←	Interrupt from CTRL 2
IRQ 8	Realtime clock interrupt
IRQ 9	Software redirected to INT 0AH (IRQ 2)
IRQ 10	Reserved
IRQ 11	Reserved
IRQ 12	Reserved
IRQ 13	Coprocessor
IRQ 14	Fixed disk controller
IRQ 15	Reserved
IRQ 3	Serial port 2
IRQ 4	Serial port 1
IRQ 5	Parallel port 2
IRQ 6	Diskette controller
IRQ 7	Parallel port 1

DIRECT MEMORY ACCESS

Eight DMA channels are supported by the system. Two Intel 8237-5 DMA controller chips (four channels in each chip) are used. DMA channels are assigned as follows:

CTRL 1	CTRL 2
Ch 0 – Spare	Ch 4 – Cascade for CTRL 1
Ch 1 – SDLC	Ch 5 – Spare
Ch 2 – Diskette	Ch 6 – Spare
Ch 3 – Spare	Ch 7 – Spare

Channels 0 through 3 are contained in DMA controller 1. Transfers of 8-bit data, 8-bit I/O adapters and 8-bit or 16-bit system memory are supported by these channels. Each of these channels will transfer data in 64KB blicks throughout the 16-megabyte system address space.

Channel 4 through 7 are contained in DMA controller 2. To cascade channels 0 through 3 to the microprocessor, use channel 4. Transfers of 16-bit data between 16-bit adapters and 16-bit system memory are supported by channels 5, 6, 7. DMA channels 5 through 7 will transfer data in 128KB blocks throughout the 16-megabyte system address space. These channels will not transfer data on odd-byte boundaries.

The addresses for the page register are as follows:

PAGE REGISTER	I/O HEX ADDRESS
DMA Channel 0	0087
DMA Channel 1	0083
DMA channel 2	0081
DMA channel 3	0082
DMA channel 5	008B
DMA channel 6	0089
DMA channel 7	008A
Refresh	008F

Address generation for the DMA channels is as follows:

* For DMA channels 3 through 0

SOURCE	AMA PAGE REGISTERS		8237A-5	
Address	A23	A16	A15	A0

Note: To generate the addressing signal "byte high enable" (BHE) invert address line A0.

* For DMA channels 7 through 5

SOURCE	DMA PAGE REGISTERS		8237A-5	
Address	A23	A17	A16	A1

Note: The BHE and A0 addressing signals are forced to a logic 0. DMA channel addresses do not increase or decrease through page boundaries (64KB for channels 0 through 3 and 128KB for channels 5 through 7).

REAL TIME CLOCK AND NONVOLATILE RAM

The real time clock MC146818 and its 64 bytes of RAM information are backed up by 6V DC battery. The internal clock circuitry uses 14 bytes while the rest is allocated to system configuration.

ADDRESS	DESCRIPTION
00	Seconds
01	Second alarm
02	Minutes
03	Minute alarm
04	Hours
05	Hour alarm
06	Day of week
07	Date of month
08	Month
09	Year
0A	Status register A
0B	Status register B
0C	Status register C
0D	Status register D
0E	Diagnostic status byte
0F	Shutdown
10	Diskette drive type byte – driver A and B
11	Reserved
12	Fixed disk type byte – driver C and D
13	Reserved
14	Equipment byte
15	Low base memory
16	High base memory
17	Low expansion memory byte
18	High expansion memory byte
19 2D	Reserved
2E 2F	2 byte CMOS checksum
30	Low expansion memory byte
31	High expansion memory byte
32	Data century byte
33	Information flags (set during power on)
34 3F	Reserved

IV. CHIPS TECHNICAL INFORMATION

PC/AT COMPATIBLE CHIP SET VL82C100/82C101/82C102/82C103/82C104

FEATURES:

* Fully compatible with IBM PC/AT-type designs
* High-Integration five-chip set
* Reduces non-memory system device count from 110 to 16
* Supports 12MHz processor clock
* Devices are available as "cores" for user-specific designs
* All devices designed in CMOS for low power consumption

82C100 PC/AT PERIPHERAL CONTROLLER

DESCRIPTION

The VL82C100 PC/AT Peripheral Controller replaces two 82C37A Direct Memory Access Controllers, tow 82C59A Interrupt Controllers, and 82C54 Programmable Counter, a 74LS 612 AT Memory Mapper, two 74ALS573 cotal three-state latches, a 74ALS138 3-to-8 Decoder, and five other less-complex integrated circuits. Using this internal functionality, the VL82C100 interfaces the keyboard controllers as well as the real time clock to the PC/AT system.

The device also supplies control signals to the I/O slots, the VL82C101 System Controller as well as the system ROMs.

The device is manufactured with VLSI's advanced high-performance CMOS process and is available in a JEDEC-standard 84-pin plastic leased chip carrier (PLCC) package.

82C101 PC/AT SYSTEM CONTROLLER

DESCRIPTION

The VL82C101 PC/AT system Controller replaces an 82C284 clock Controller and 82C288 Bus Controller (both are used in 286-based systems), an 82C84A Clock Generator and Driver, two PAL16L8 devices (used for memory decode), and approximately ten other less-complex integrated circuits used as Wait State logic. When used in 12MHz systems utilizing 80ns DRAMs, the device provides the required one wait state for a "write" operation, and zero wait states for a "read" operation. A 12MHz system using 120ns DRAMs will be provided with one wait state for "write" and one wait state for a "read". The device accepts both the 24MHz crystal to control the system clock as well as the 14.318MHz crystal to control the microprocessor clock. It also supplies reset and clock signals to the I/O slots. The device is manufactured with VLSI's advanced high-performance CMOS process and is available in a JEDEC-standard 84-pin plastic leaded chip carrier (PLCC) package.

82C102 PC/AT MEMORY CONTROLLER

DESCRIPTION

The VL82C102 PC/AT Memory controller generates the row address strobe (RAS) and column address trobe (CAS) necessary to support the dynamic RAMs used in the PC/AT. Inaddition, the device allows four motherboard memory options for the user, up to a full 2M-byte system. Three of the four options allow a full 640K-bytes user area to support the disk operating system (DOS). In addition, the VL82C102 provides the upper addresses to the I/O slots, the chip select for the ROM and RAX memory, and drives the system's speaker.

The device is manufactured with VLSI's advanced high-performance CMOS process and is available in a JEDEC-standard 84-pin plastic leaded chip carrier (PLCC) package.

82C103 PC/AT ADDRESS BUFFER

DESCRIPTION

The VL82C103 PC/AT Address Buffer provides the system with a 16-bit address bus input and 41 buffered drivers. The buffered drivers consist of 17 bidirectional system bus drivers each capable of sinking 20mA (50 'LS loads) of current and 200 picofarads of capacitance on the backplane; 16 bidirectional local bus drivers, each capable of sinking 80mA (20 'LS loads) of current; and eight memory bus drivers, also capable of sink-

ing 8mA of current on-chip refresh circuitry supports both 256K-bit and 1M bit DRAMs. The VL82C103 provides addressing for the I/O slots as well as the system.

The device is manufactured with VLSI's advanced high-performance CMOS process and is available in a JEDEC-stand 84-pin plastic leaded chip carrier (PLCC) package.

82C104 PC/AT DATA BUFFER

DESCRIPTION

The VL82C104 PC/AT Data Buffer provides a 16-bit data bus input as well as 40 buffered drivers. The buffered drivers consist of 16 bidirectional system data bus drivers, each capable of sinking 20mA (50 'LS loads) of current; eight bidirectional local bus drivers, each capable of singing 8mA (20 'LS loads 0 of current; and 16 memory data bus drivers, each capable of sinking 8mA (20 'LS loads) of current. The VL82C104 also generates the parity error signal for the system.

The device is manufactured with VLSI's advanced high-performance CMOS process and is available in a JEDEC-standard 84-pin plastic leaded chip carrier (PLCC) package.

V. HOW TO CONTROL THE SYSTEM SPEED BY SOFTWARE

1. Press "CTRL", "ALT" and " -" to change speed
   or press "CTRL", "ALT" and "+" to change speed

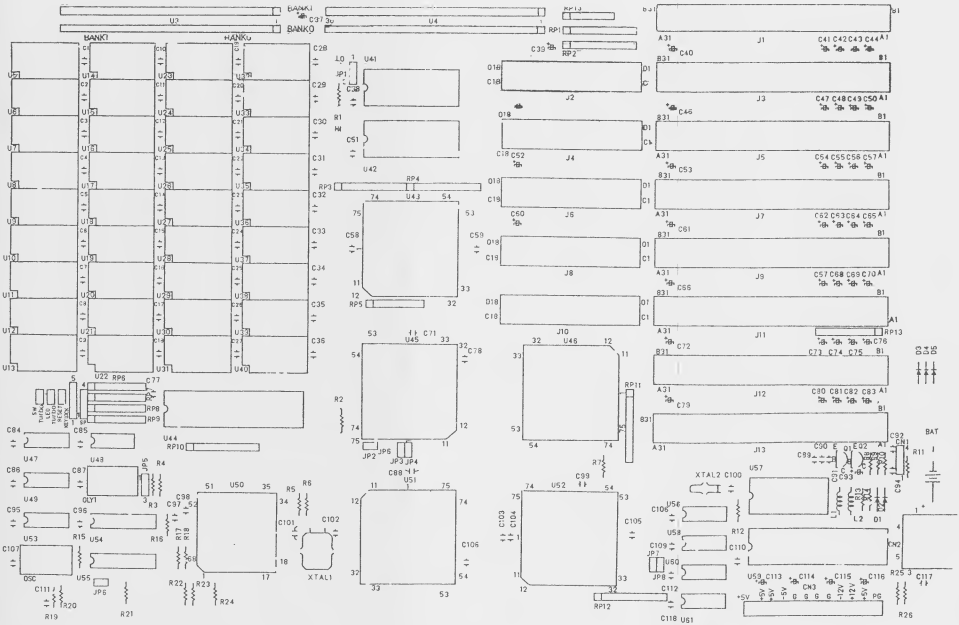
   A: <ALT>
   C: <CTRL>
   S: <SHIFT>
   –: < – > –
   +: < + >

2. When the equipment of mainboard used AWARD BIOS and PTC 8042 Controller

   A: < ALT >
   B: < CTRL>
   –: < – >
   +: < + >

3. When the equipment of mainboard used AMI BIOS

   A: < ALT >
   B: < CTRL>
   C: < \ > slash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BANK0
U2
U4
J1
J2
J3
J4
J5
J6
J7
J8
J9
J10
J11
J12
J13
U41
U42
U45
U46
U50
U51
U52
U57
U61
RP1
RP2
RP3
RP4
RP5
RP6
RP7
RP8
RP9
RP10
RP11
RP12
RP13
JP1
JP2
JP3
JP4
JP5
JP6
JP7
JP8
OSC
XTAL1
XTAL2
BAT
CN1
CN2
CN3
+5V
PG